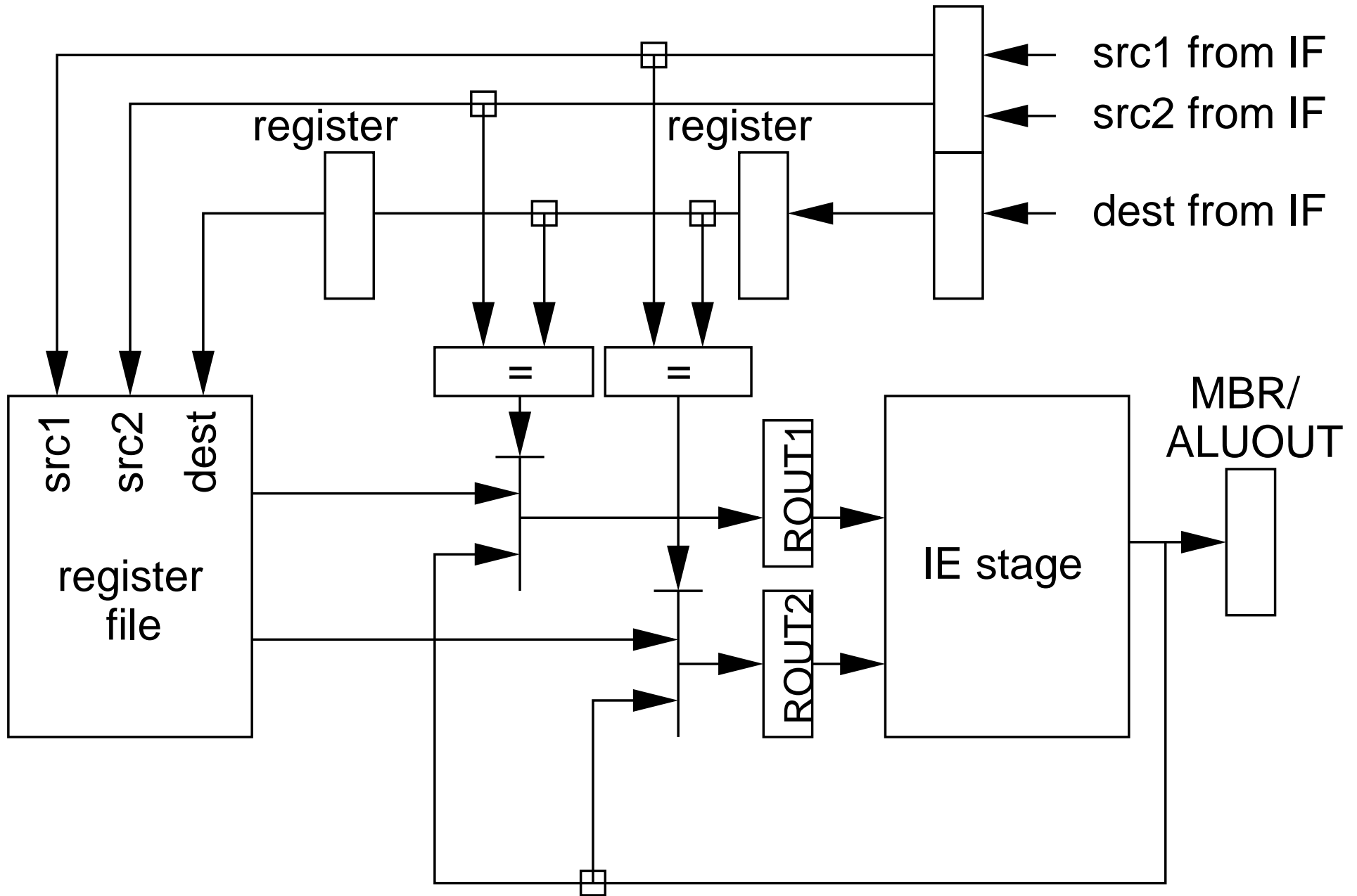
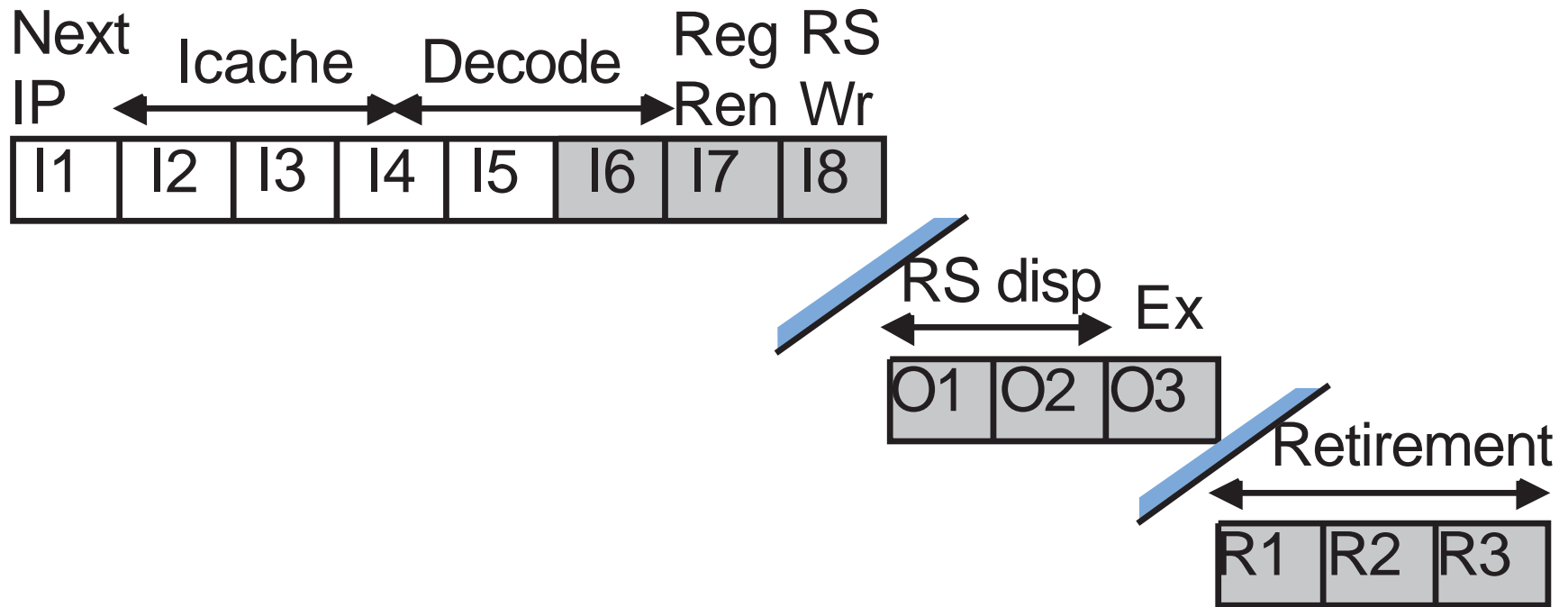


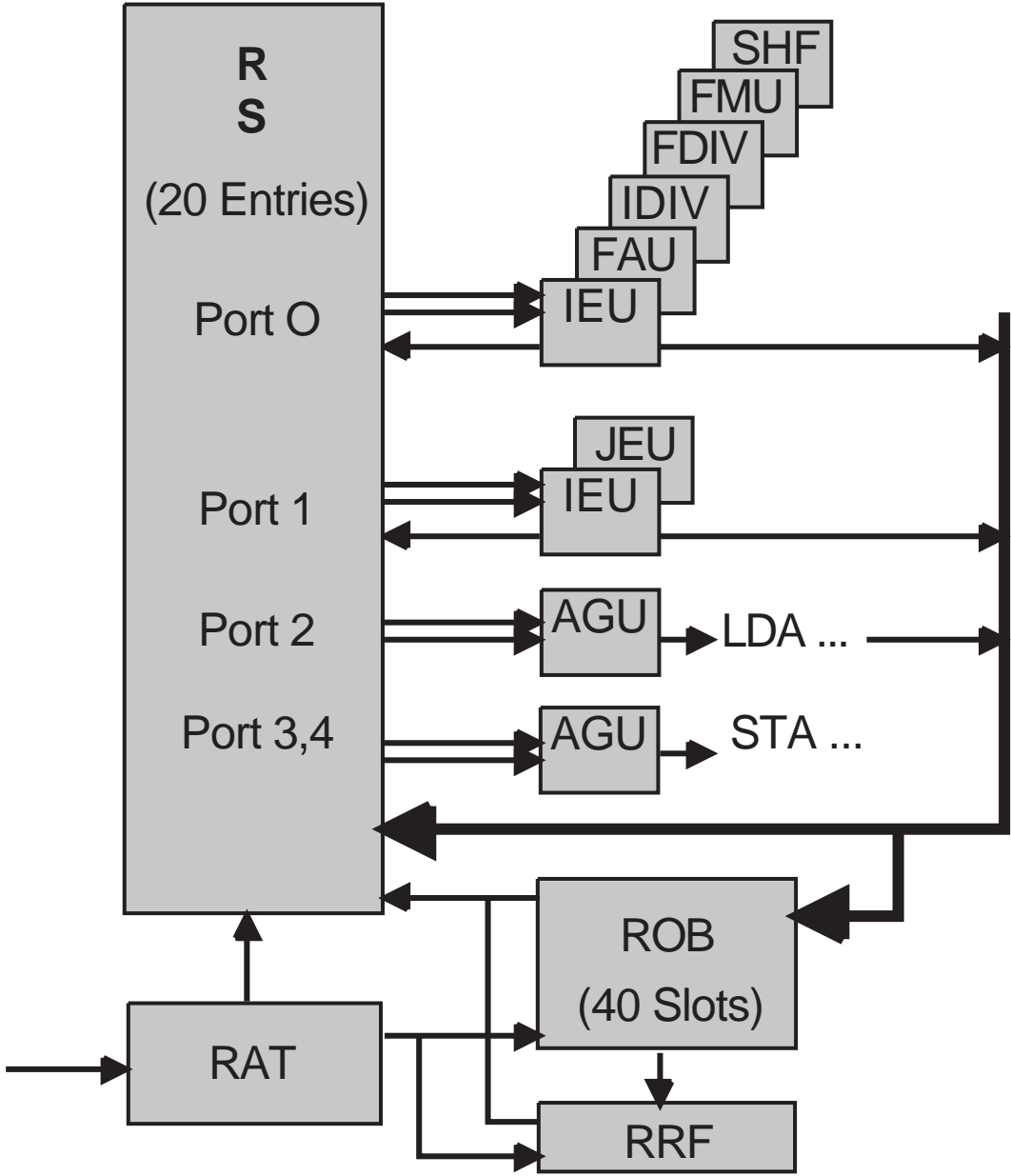
Bypassing Hardware



Example Pipeline



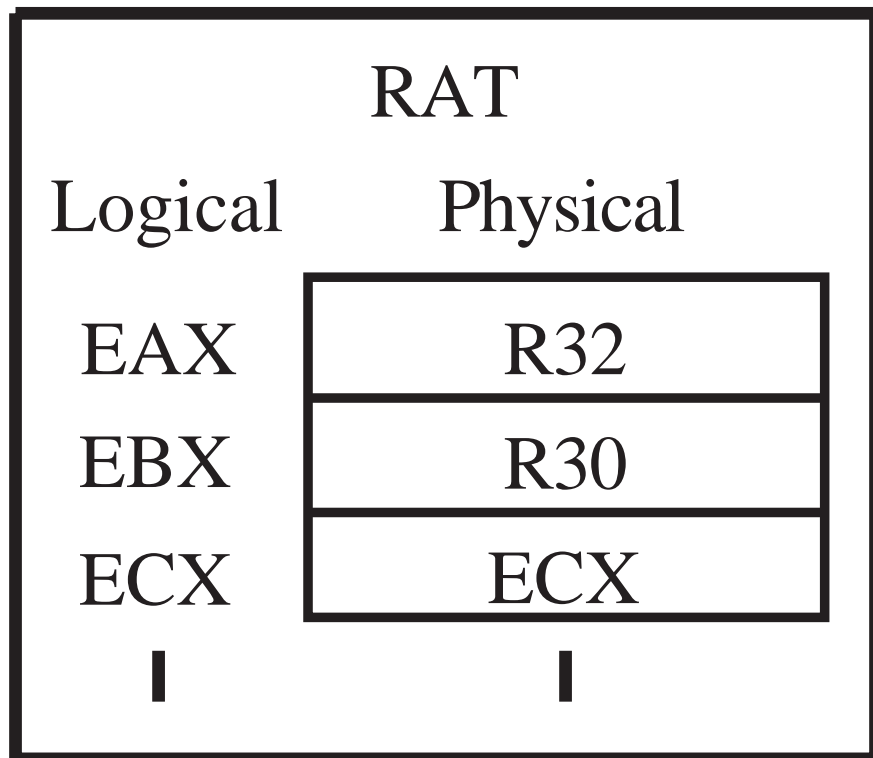
OOO Core



Register Alias Table

RAT	
Logical	Physical
EAX	R32
EBX	R30
ECX	ECX
I	I

Register Renaming: Step 1

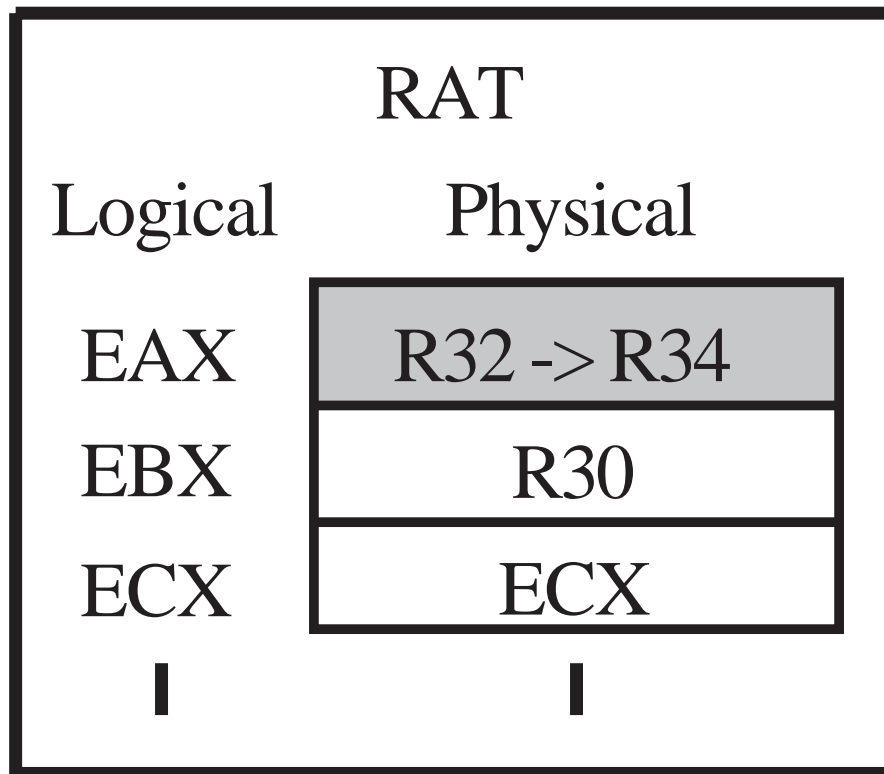


EAX \leftarrow EAX + EBX
EAX \leftarrow EAX + ECX



EAX \leftarrow R32 + R30
EAX \leftarrow R32 + ECX

Register Renaming: Step 2

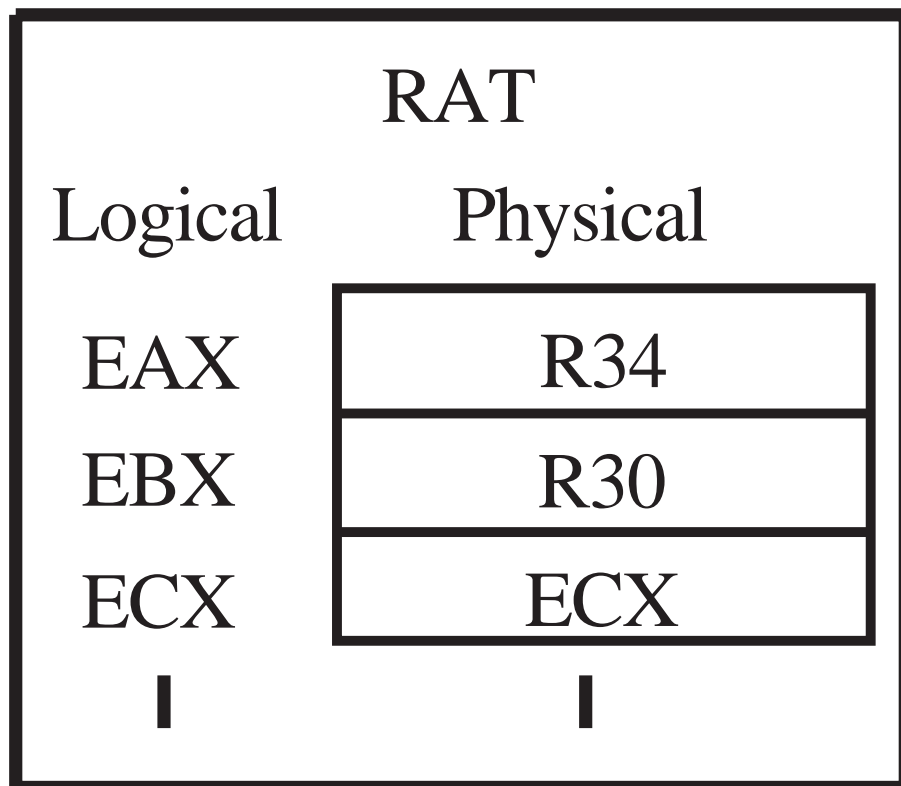


$EAX \leftarrow R32 + R30$
 $EAX \leftarrow R32 + ECX$



$R33 \leftarrow R32 + R30$
 $R34 \leftarrow R32 + ECX$

Register Renaming: Step 3

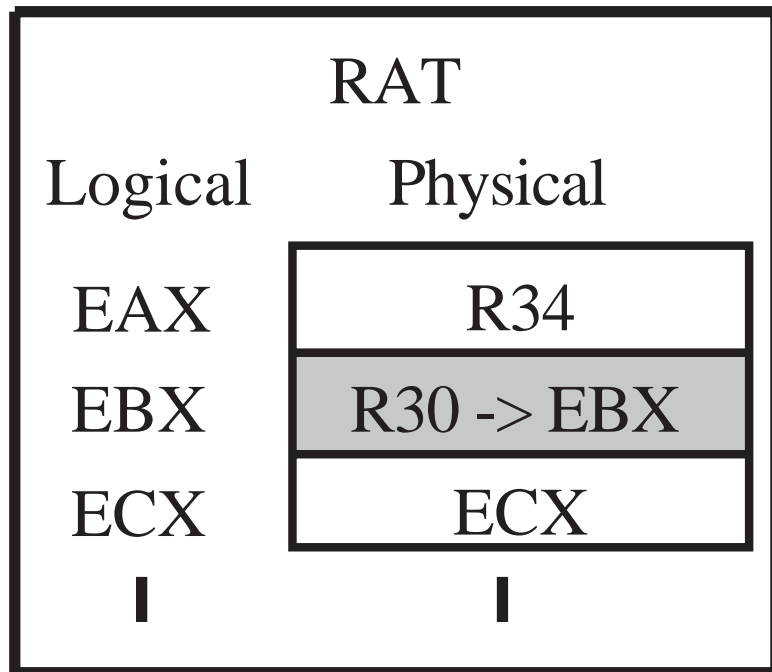


$R33 \leftarrow R32 + R30$
 $R34 \leftarrow R32 + ECX$



$R33 \leftarrow R32 + R30$
 $R34 \leftarrow R33 + ECX$

Register Renaming: Step 4



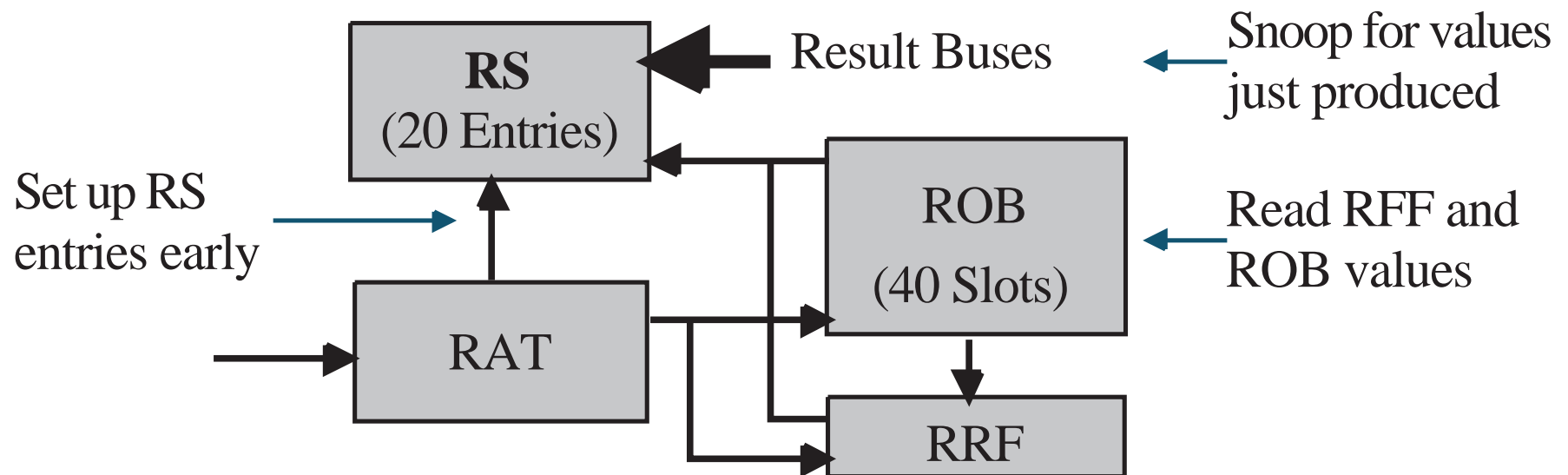
R33 <- R32 + R30
R34 <- R33 + ECX

Retired:
R29 -> EAX
R30 -> EBX



R33 <- R32 + EBX
R34 <- R33 + ECX

Reservation Station



Reservation Station Entries

V	Opcode	Src1			Src2			Dest Reg
		Reg	Value	V	Reg	Value	V	
1	add	R32	12	1	EBX	34	1	R33
1	add	R33	--	0	ECX	56	1	R34
0								
0								

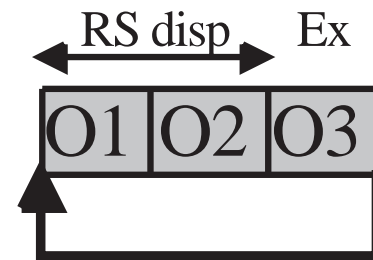
← R33 ← R32 + EBX

← R34 ← R33 + ECX

Dispatch 1

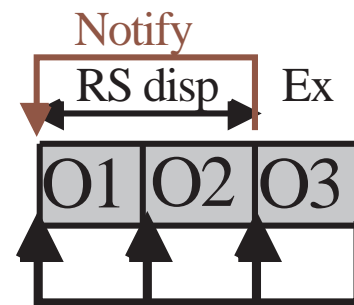
R33 \leftarrow R32 + EBX

R34 \leftarrow R33 + ECX



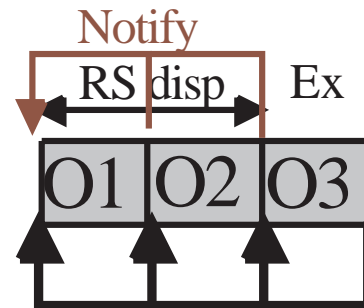
R33 \leftarrow R32 + EBX

R34 \leftarrow R33 + ECX

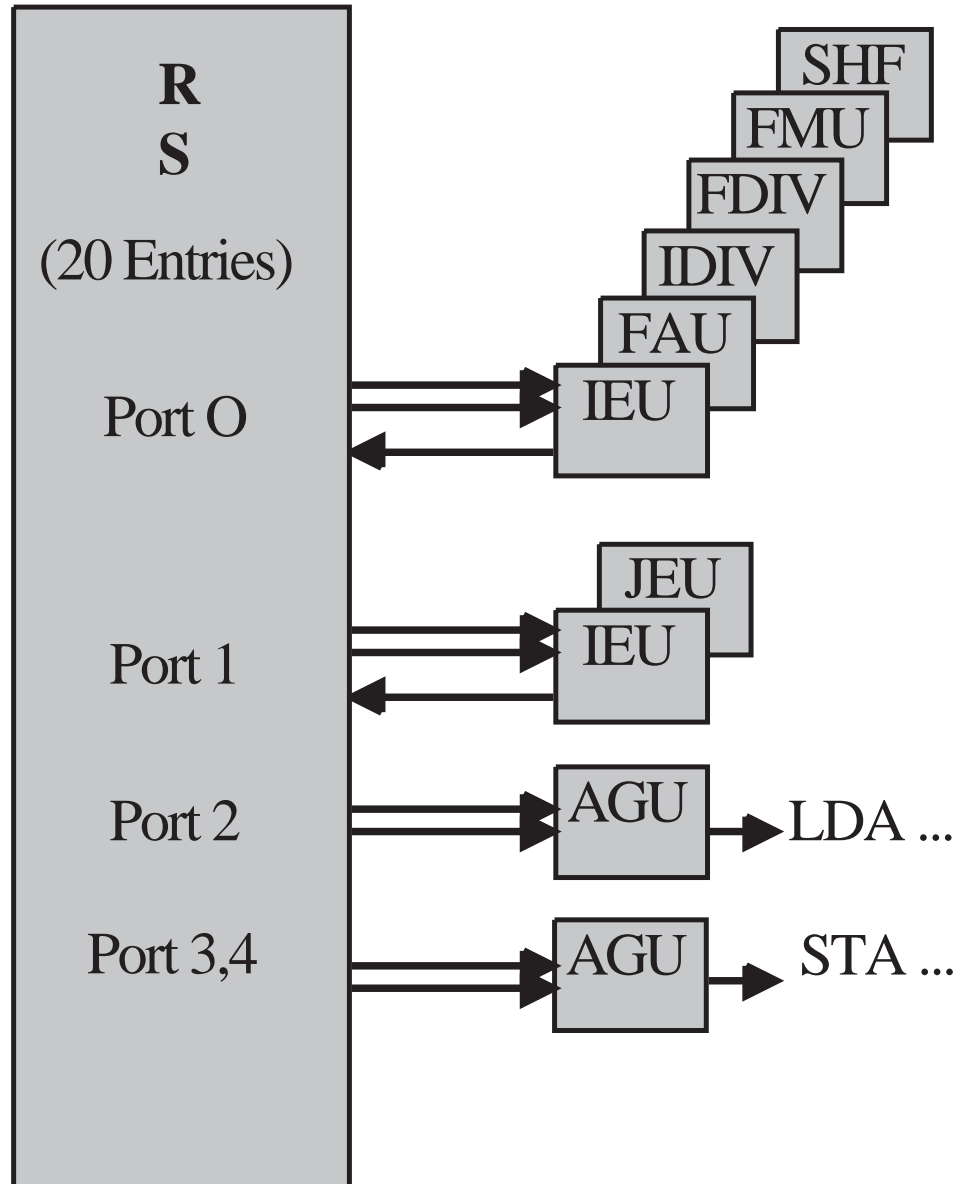


Dispatch 2

R33 \leftarrow R32 + EBX
R34 \leftarrow R33 + ECX



Dispatch Port Selection



Maintaining Precise State

	Comp Exec	Exec Flags	RRF Dest	Value
	1	1	1	1
R33	1	--	EAX	46
R34	0	--	EAX	--
R35	1	mp	--	CB10
R36	1	invadr	EAX	--
	1	1	1	1

← R33 ←- R32 + EBX

← R34 ←- R33 + ECX

← JMP CB10 ← Mispredicted br.

← R36 ←- MEM[ECX]

Excepting speculative LD

Fixing Mispredicted Branches

	Comp Exec	Exec Flags	Dest RRF	Value	
R33	1	--	EAX	46	← R33 ← R32 + EBX
R34	0	--	EAX	--	← R34 ← R33 + ECX
R35	1	mp	--	CB10	← JMP CB10
R36	1	invadr	EAX	--	← R36 ← MEM[ECX]

