
UIUC ECE 512

Course Introduction

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Outline

- Syllabus
 - www.crhc.uiuc.edu/ece411
- Background and motivation
- Overview of technical contents

Contact Information

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 - Office Hours: 2-3 M/W
- Students
 - see syllabus for details
 - submit by 3rd lecture

Textbooks

- Required
 - Class notes, Spring 2005
 - Reading, Spring 2005
- Recommended
 - TBD.

Grading

- Exam - 40%
 - lectures and reading
- Project Report - 30%
 - proposal and final report
 - technical and presentation

Grading (cont.)

- Project Presentation - 20%
 - technical, organization, oral, Q&A
- Class Participation - 10%
 - questions, comments, suggestions
 - in class or e-mail

Class Project

- Team of two to three
- Stage 1 - one-page proposal
 - see syllabus for suggested topics
 - identify 10 papers
 - relation to course objectives
 - well beyond reading and lectures
 - due at the 11th lecture

Class Project (cont.)

- Stage 2 - report and presentation
 - 5-10 pages, double columned
 - due at the 25th lecture
 - 15-30 min. oral presentations
- Focus - learning, not publication

Computer Microarchitecture

- The art of organizing logic level components to implement a computer.
- Traditional layers of abstraction
 - algorithm, languages, **compiler**, **ISA**, **u-arch**, circuit, u-electronics
- Cross-cutting design fact of life

Why is uArch Important

- Computers are everywhere
 - servers, desktops, laptops, set-tops, appliances, machinery, vehicles, toys, devices, etc.
- Any future innovations likely involve computer design
 - performance, cost, power, size, reliability, new circuit/technology

Why is uArch Interesting

- Sizable amount of transistors
 - Fabrication technology enables low cost multi-million-transistor chips.
- Demanding applications
 - New, ambitious applications demand more ambitious hardware design and software technology

Focus of the Course

- uArch and compiler techniques for current and future
 - CPU microprocessors
 - DSP/embedded microprocessors
 - Application specific IP blocks
 - System on a chip solutions

X86 Microprocessors

- Very large volume
- Intel dominates, AMD follows
 - examples: Celeron, K6-2
- Critical aspects
 - windows compatibility
 - multimedia and game support
 - chipset and standards

Server Microprocessors

- Enterprise and scientific/engineering applications
 - HP, SUN, Compaq, IBM (ex.)
 - Unix, Linux, Win/NT
 - consolidating to IA-64 and Power
 - multiprocessor support important
 - small volume but high margin

Embedded Microprocessors

- Very large volume, low margin
- Motorola (ex.), Intel, ARM, ST dominate
- Critical aspects
 - low total system cost
 - low power
 - work with ASIC's and standards

DSP microprocessors

- Very large market, low margin
 - disk drives, modems, wireless, etc.
 - TI, Lucent, Motorola dominate
- Critical aspects
 - very high throughput
 - low cost, low power
 - integration with control (ex.)

System on a chip

- Complete solution on a chip
 - lower cost and power than boards
- Many contenders, e.g., National
- Critical aspects
 - IP licensing and interfacing
 - interconnects
 - verification and test

Technical Content

- Instruction fetch and decode
 - branch prediction
 - instruction cache design
 - wide fetch mechanisms
 - variable instruction format

Technical Content (cont.)

- Execution scheduling and opti.
 - Instruction issue
 - register bypass/forwarding
 - register renaming
 - interlocking
 - out-of-order execution
 - basic compiler techniques

Technical Content (cont.)

- EPIC architecture and compiler
 - explicit parallelism
 - control and data speculation
 - predicated execution
 - if-conversion, decision framework
 - predicate analysis and data flow
 - predicate optimization
 - recovery models

Technical Content (cont.)

- Data cache and memory system
 - streaming and buffering
 - intelligent cache management
 - memory system organization
 - high speed DRAM interfaces
 - memory access ordering

Technical Content (cont.)

- Install-time and run-time opti.
 - Compiler support
 - binary analysis
 - optimization opportunities
 - run-time profiling techniques
 - run-time optimizations

Technical Content (cont.)

- Domain specific u-architectures
 - traditional DSP architecture
 - X-Y memory, MAC, circular buffers, saturating arithmetic, etc.
 - VLIW/EPIC DSP
 - network processors
 - 3D graphics
 - accelerators

Technical Content (cont.)

- Case studies
 - X86 CPU: P3/P4, K6/K7
 - RISC CPU: Alpha 21264
 - EPIC CPU: IA-64
 - Trad. DSP: TI C40, Lucent 56000
 - EPIC DSP: TI C60, Motorola/
Lucent StarCore