UIUC ECE 512 Course Summary

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ECE

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Basic Lectures

- Processor
  - I-Fetch
  - OoO
    - Renaming, Scheduling
    - State recovery
  - VLIW/EPIC
    - Trace, superblock, hyperblock
    - Modulo scheduling
    - Control and data speculation
    - Predication
- Memory System
  - DRAM, SDRAM, DDR-SDRAM, R-DRAM, tec.
- Application Specific
  - Common DSP ISA features, design examples

Your presentations

- Reality of OoO Design
- Reality of EPIC Design
- Power efficient design
- Dynamic Optimization
- Multicore Programming
- Reconfigurable Computing
- Fabrication Technology
- Application specific Designs

Grading

- Exam - 40%
  - lectures and reading
- Project Report - 30%
  - proposal and final report
  - technical and presentation

Grading (cont.)

- Project Presentation - 20%
  - technical, organization, oral, Q&A
- Class Participation - 10%
  - questions, comments, suggestions
  - in class or e-mail