

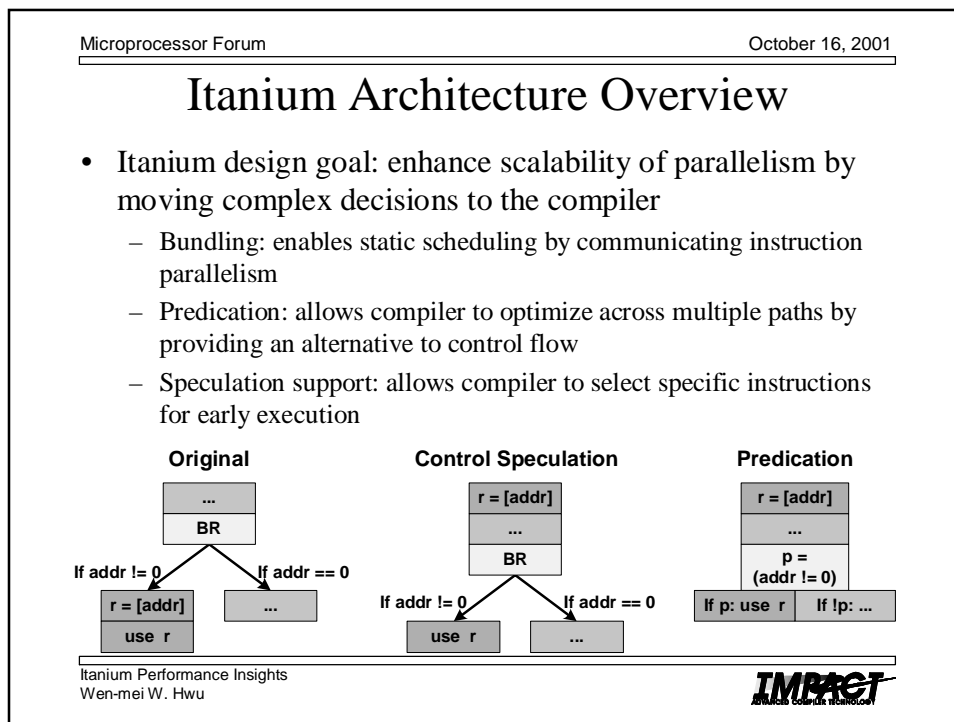
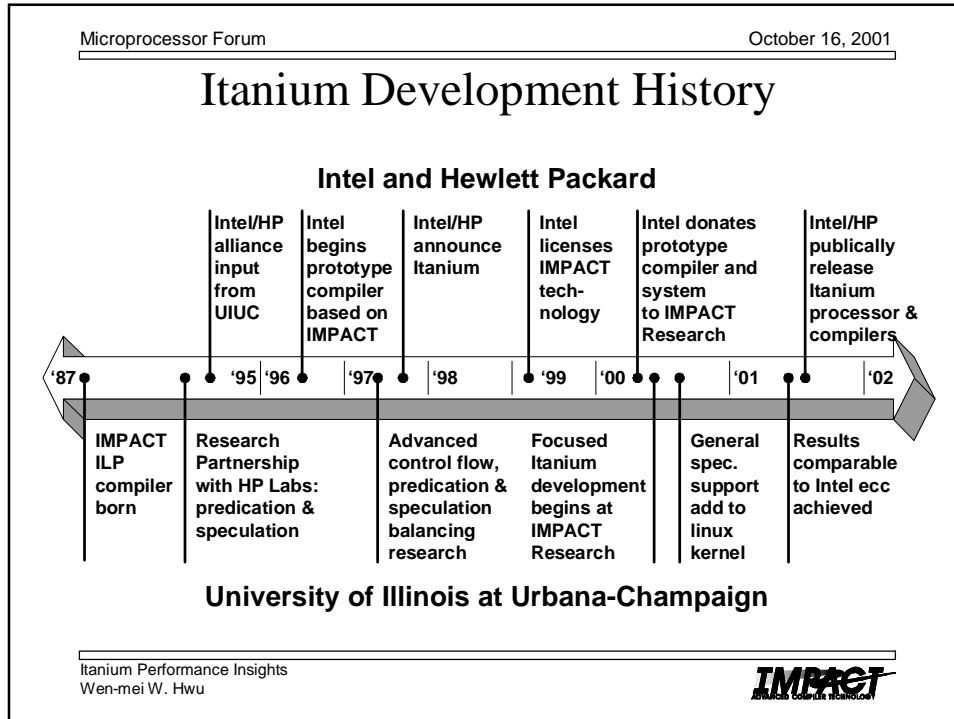
# Itanium™ Performance Insights

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## Predictions from MPF 1998

- Compilers critical to the performance of EPIC uP's
  - Use of predication and speculation is a serious challenge.
  - Any misuse will lead to performance loss.
  - Brand new algorithms will be deployed in the EPIC compilers.
  - Existing software development models must be supported.
- Expect performance robustness issues
  - Awesome performance leap seen for some applications.
  - Less for others due to limitations of analyses and optimizations.
  - It can take years for the performance gain to be universal.
- Evolution of EPIC architectures
  - Revisions of architectures are likely as compilers mature.
  - Code size and power consumption are critical for embedded EPICs.
- After three years...what is the reality?



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## Itanium Compilation Landscape

- Increased reliance on the compiler for performance
  - Explicit control of the architecture: realities of modern microarchitecture have become visible at software level
  - Particular problems: effects of runtime uncertainty
    - Control resolution, variable memory latency, etc.
  - Solutions from EPIC/VLIW research
    - Memory disambiguation, profiling
    - Static scheduling, control speculation, predication

	Application coverage	Public/Proprietary	Peephole opti level	ILP opti level	Extensibility	Mode
GNU gcc	Very High	Public	Low	Very Low	Low	LP64
Intel ecc	High	Proprietary	High	High	High	LP64
HP aCC	High	Proprietary	High	High	High	ILP32
IMPACT	Medium	Future Public	Medium	Very High	Very High	LP64

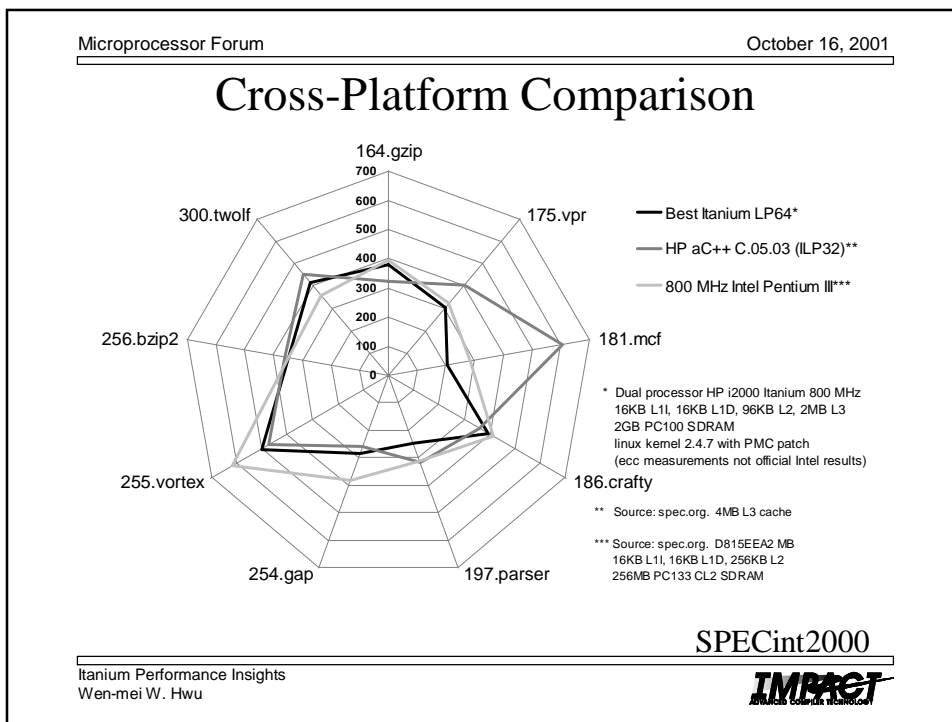
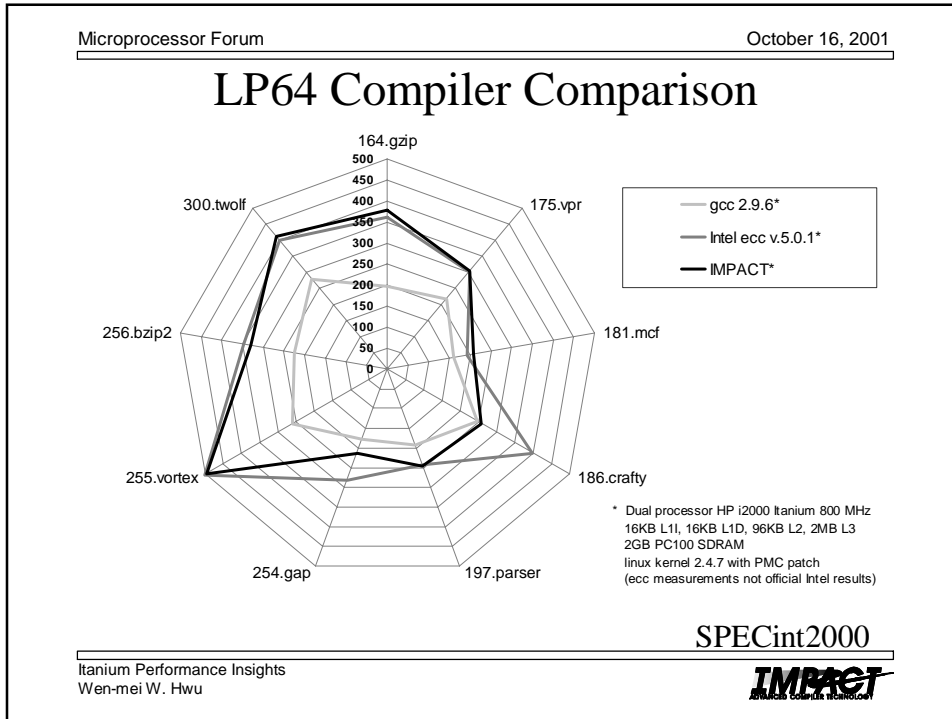
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## IMPACT Compiler

- IMPACT compiler supports ILP compilation and research
  - Extensible framework for easy implementation of new optimizations
  - Versatile and pervasive intermediate representation (IR)
  - Advanced interprocedural pointer analysis
  - Comprehensive predicate-aware dataflow and predicate analyses
  - Direct analysis from IR at most stages of compilation

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### Ex: 175.vpr route\_net() (SPECcpu2000)

- Base optimizations: function inlining, hyperblock formation, and loop unrolling
- Aggressive redundant load and operation elimination (red) [saves 18 cycles of 65]
- Advanced pointer analysis could disambiguate loads and stores (green) [save 5 additional cycles]

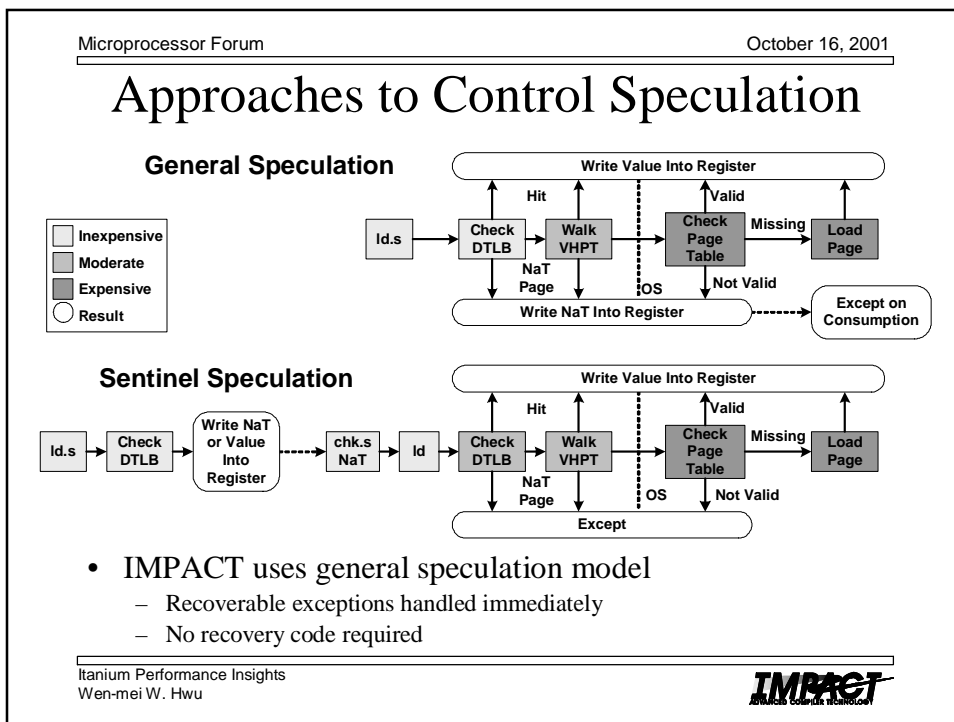
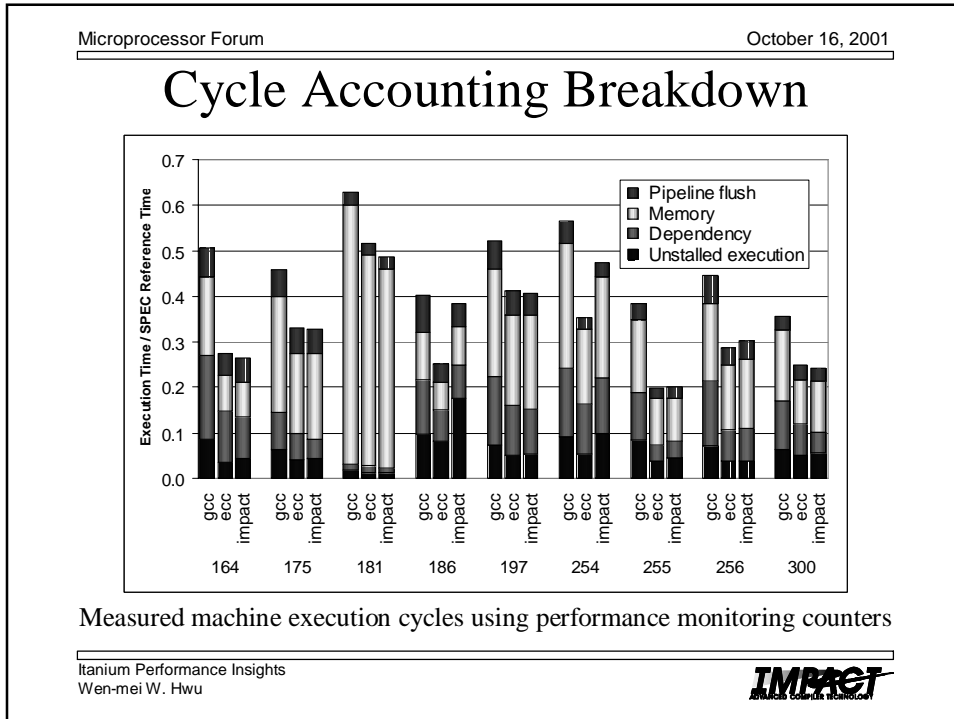
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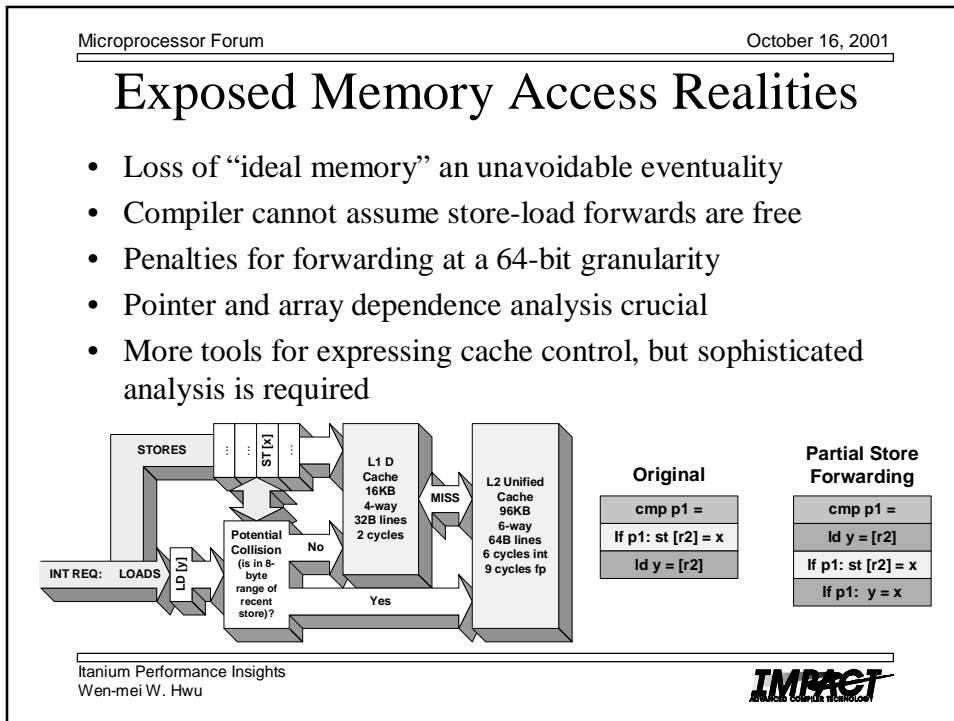
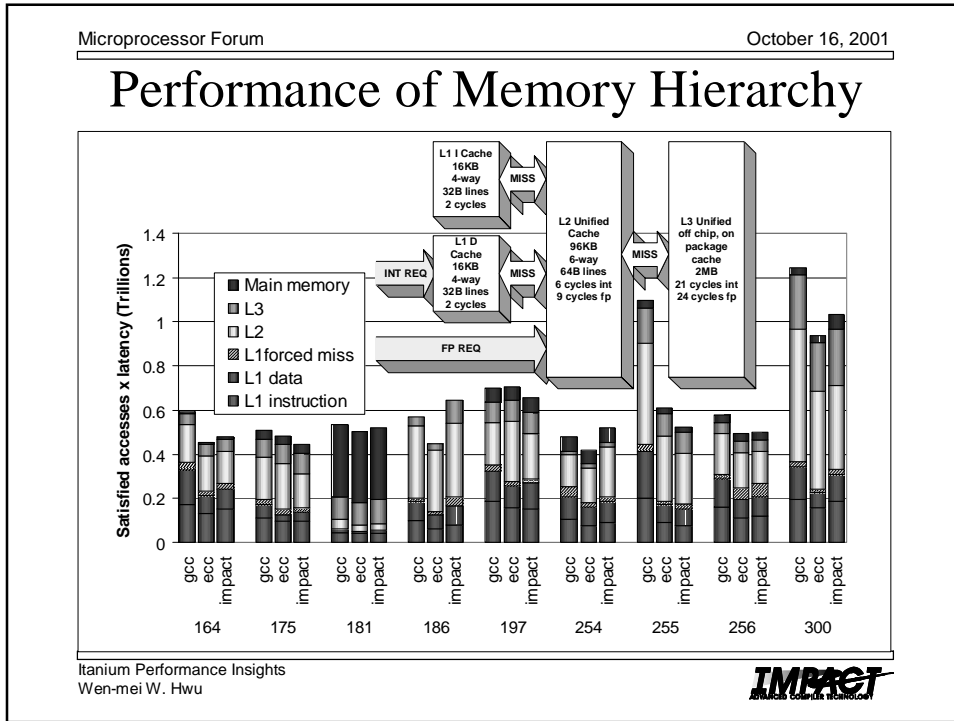
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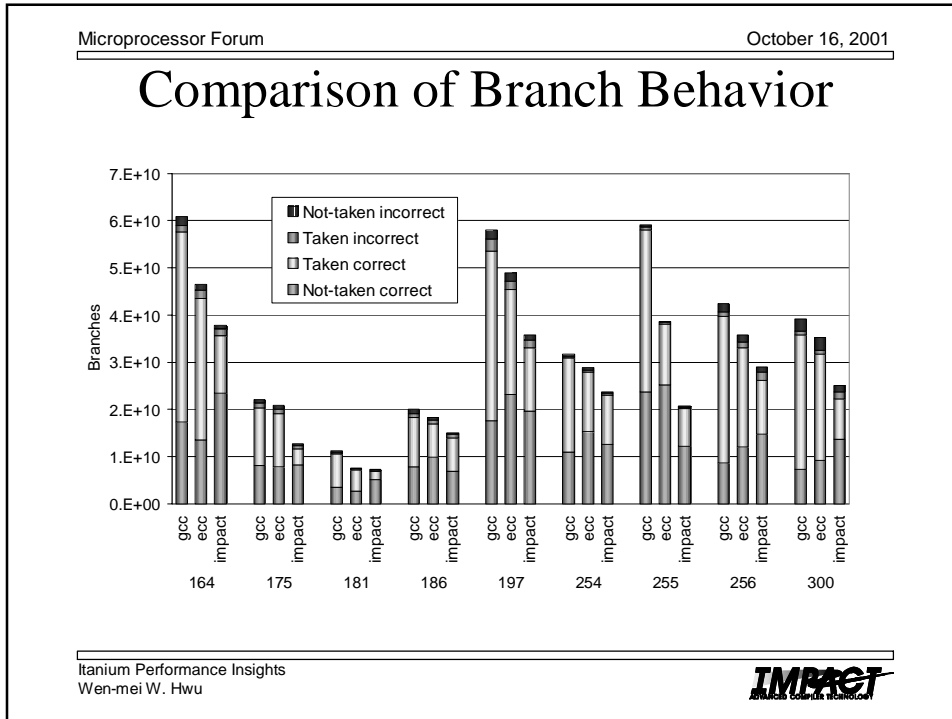
### IPC and EPIC Instruction Issue

- Available ILP varies widely
- Bundling moderates between code size and efficient parallel issue

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- ## Reflections and Projections
- Compiler integral part of performance
    - Itanium benefits substantially from carefully targeted optimization
    - Brand new algorithms will be deployed in the EPIC compilers
    - Existing software development models must be supported / augmented
  - Today, a mix of mature and immature compiler technologies
    - First Itanium machines and compilers are competitive at par frequency
    - High performance on particular benchmarks
    - Targeted optimization of memory access required for performance growth
    - Performance monitoring hardware provides guidance, assessment
  - Evolution of EPIC architectures
    - Revisions of architectures are likely as compilers mature and microarchitectures become more exposed
    - Opportunities extend into load-time and run-time optimizations
  - Significant performance headroom in product compilers
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